



INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
MATERIALS MANAGEMENT DIVISION
Powai, Mumbai 400076.

Ref. PR No. 1000051204

Rfx. No. 6100002696

Item Description : Consultancy for Field-Programmable Gate Array Prototyping Services (FPGA)

Sr. No	Item Description	Detailed Technical Specification	Technical Compliance (Yes / No)	Additional Information (if any)
1.	Select FPGA	Scope of Work : Identification of the FPGA card in consultation with IITB		
2.	Configure Ethernet MAC IP	FPGA block reference design with MAC IP from FPGA vendor integrated with Ethernet PHY on the FPGA board. The achieved data transfer rate should be at least 80% of the peak rate offered by the interface (1G or 10G). Interfacing to, and software drivers for the host computer should also be developed for further use		
3.	Configure PCIe Endpoint IP	FPGA block reference design with PCI-e endpoint IP from FPGA vendor integrated with PCI-e PHY on the FPGA. The achieved data rate must be at least 80% of peak provided by the interface. Interfacing to, and software drivers for the host computer should also be developed for further use.		
4.	Configure DDR Controller IP	FPGA block reference design with DDR Controller IP from FPGA vendor integrated with external DDR3 DRAM on the FPGA board		

5.	Integrate Interface block (Ethernet MAC IP, PCIe IP, Switch, DMA Controller and DDR Controller)		
6.	Integrate Interface block with SoC Core		
7.	Bring-up PCIe Interface and establish communication to SoC Core		
8.	Bring-up Ethernet Interface and establish communication to SoC Core		
9.	Support Full SoC Bring-up Assistance to the IITB team in the bring-up of the SOC prototype on the FPGA card		
10.	Payment Terms : The Payment will be made after completion of each milestone subject to satisfactory certification by indenter.		
11.	Milestone Criteria : i. Map Sample RTL (VHDL) of the AJIT processor from IITB to existing Xilinx FPGA board at IITB (Completion Period : 2 weeks from the date of PO.) ii. Map processor + accelerator (1+1 configuration) to existing high-capacity Xilinx board at IITB & demonstrate communication between board & host. (Completion Period : 5 weeks from the date of PO.)		